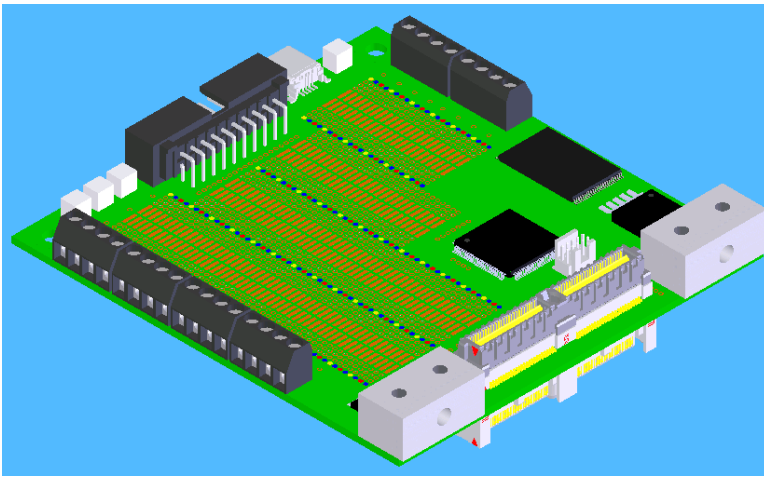




UFC-3 OPEN SYSTEM DEVELOPER'S MODULE



Now the high performance Universal Flight Controller (UFC-3) modular rocketry avionics system is truly Universal with the introduction of the Open System Developer's (OSD) Module.

Individuals, colleges and universities, and small companies can now implement custom avionics at low cost and shortened development time when building upon the UFC modular system.

Features

- Standard UFC Module form factor and electrical interface (Plug and Play)
- Able to monitor or control any UFC Module
- Communicates directly with UFC CPU
- Supports hardware redundancy control
- Free development tools by Cypress Semiconductor (only \$90 for required programming/debug pod)
- Tested hardware/software design templates for all UFC interface functions; UART, SPI, Digital I/O, etc
- Black Magic Support

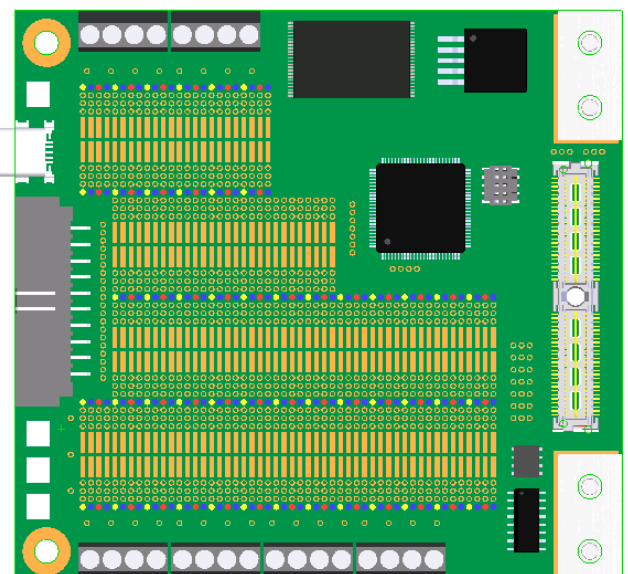
Benefits

- Builds upon wide variety of established modules; CPU, Telemetry, GPS, Inertial Sensor, ADC, Power Output
- No need to develop/test common avionics functions
- Provides gateway to other UFC functions
- Maintains high reliability fault tolerant system
- Well supported development tools including on-line technical support from Cypress
- User can focus on their design task and easily link in with UFC functions
- We assist you in completing your project and packaging your design if desired

User defined hardware inside and out:

The bread-boarding area allows expansion of user defined digital/analog functions programmed into the Cypress PSoC 5 chip. It supports a variety of SOIC/0603 components, user supplied USB, 20-pin IDC and screw terminal connectors, buffered LEDs and optional NAND Flash. Choice of 3.3VDC and/or 5VDC power supplies.

Black Magic can turn the user's prototype design into a fully manufacturable, rugged assembly at minimal cost and with quick turn around.



Presenting UFC-3 Open System Developer's Module

- Cypress PSoC 5 (CY8C55) Programmable System-on-Chip including:
 - 80 MHz ARM Cortex-M3 32-bit RISC processor
 - 256KB of Flash Memory
 - 64KB of SRAM
 - 2KB of EEPROM
 - CAN 2.0b
 - USB 2.0 (external or one of two stack connections)
 - I²C Master
 - Four 16-bit timer/counter/PWM blocks
 - 24 programmable PLD based Universal Digital Blocks
 - May be programmed in Verilog
 - Schematic design entry
 - Configurable Macros from Libraries
 - User defined Library Macros (Component Author)
 - Library of standard digital peripherals
 - 8, 16, 24 and 32-bit timers/counters/PWMs
 - SPI
 - UART
 - I²C
 - Library of advanced digital peripherals
 - Cyclic Redundancy Check (CRC)
 - Pseudo Random Sequence generator
 - LIN Bus 2.0
 - Quadrature decoder

- Library of analog peripherals
 - 1.024V, $\pm 0.1\%$ reference
 - 12-20-bit Delta-Sigma ADC
 - Four 12-bit SAR ADC
 - 24-bit fixed point digital filter block (FIR/IRR filters)
 - Four 8-bit IDACs or VDACS
 - Four Comparators
 - Four Op Amps with 25 ma drive capability
 - Four multifunction analog blocks (PGA, TIA, Mixer, Sample and Hold, etc)
- Complete Hardware/Software design and debugging tools (MiniProg3 programming/debug adapter available for \$90 through distribution)
- Bread-boarding area for 0603/SOIC components
- USB, 20-pin IDC and screw terminal connector locations
- NAND Flash land pattern to support up to 8GB of local non-volatile memory (user supplied)
- User defined LEDs (3 user supplied)
- Complete schematics
- Design templates for UDB interface to the UFC-3 stack signals (UARTs, SPI, digital I/O ports)
- Source code for module initialization in the UFC-3 environment (communication with the Base Module)
- Synchronized with the Base Module ARM9 processor and able to exchange information, status and commands

| Alias | Name | Pin | Lock |
|-------|----------|--------|-------------------------------------|
| | I2C_SDA | P12[1] | <input checked="" type="checkbox"/> |
| | I2C_SCL | P12[0] | <input checked="" type="checkbox"/> |
| | TXD0 | P6[2] | <input checked="" type="checkbox"/> |
| | RXD0 | P6[3] | <input checked="" type="checkbox"/> |
| | RXD1 | P15[4] | <input checked="" type="checkbox"/> |
| | RXD2 | P15[5] | <input checked="" type="checkbox"/> |
| | SPI_MOSI | P4[1] | <input checked="" type="checkbox"/> |
| | SPI_CS0N | P4[7] | <input checked="" type="checkbox"/> |
| | SPI_CS2N | P4[6] | <input checked="" type="checkbox"/> |
| | SPI_CS1N | P4[5] | <input checked="" type="checkbox"/> |
| | SPI_CS0N | P4[4] | <input checked="" type="checkbox"/> |
| | SPI_SCLK | P4[2] | <input checked="" type="checkbox"/> |
| | SPI_MISO | P4[3] | <input checked="" type="checkbox"/> |
| | EM_I01 | P6[0] | <input checked="" type="checkbox"/> |
| | IO_23 | P2[0] | <input checked="" type="checkbox"/> |
| | IO_1 | P5[4] | <input checked="" type="checkbox"/> |
| | IO_2 | P12[7] | <input checked="" type="checkbox"/> |
| | IO_3 | P12[6] | <input checked="" type="checkbox"/> |
| | IO_4 | P1[7] | <input checked="" type="checkbox"/> |
| | IO_5 | P1[6] | <input checked="" type="checkbox"/> |